Notice of Allowability	Application No.	Applicant(s)	
	09/723,348	LINK ET AL.	
	Examiner	Art Unit	
	Minh Dinh	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *examiner's amendment on 12/23/05*.

2. ☒ The allowed claim(s) is/are *1-7, 9-26, 29-31,33-36*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

THOMAS R. PEESO
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jon Gibbons on 12/23/05.

The claims have been amended as follows:

1. (**Amended**) A system including an electronic device containing protected data, the electronic device comprising:

a local processor;

memory protection logic operable to interface with memory for accessing protected data stored therein, wherein access to said protected data is restricted for access by said local processor for execution thereon within ~~said~~ the electronic device;

validation logic, operative in a first mode and a second mode, for checking the validity of said protected data and for producing a validity signal to ~~determine~~ indicate whether said protected data is valid, said validation logic being accessible from ~~the~~ outside of the electronic device for setting the electronic device into one of said first mode and said second mode;

validity signal output control logic for inhibiting an output of said validity signal to outside ~~said~~ the electronic device while in said first mode, the electronic device remaining in said first mode until the validity of a predetermined quantity of said protected data has been checked;

a system reset function for resetting the system including at least said local processor; and

a device reset function for resetting said ~~validation logic~~ validity signal in response to said system being reset while the electronic device is in said first mode,

wherein said device reset function does not reset said validity signal in response to said system being reset while the electronic device is in said second mode.

8. **(Canceled)**

20. (**Amended**) A method of protecting data contained in memory of an electronic device of a system, the method comprising:

coupling memory protection logic to interface with memory for accessing protected data stored therein, wherein access to said protected data is restricted for access by ~~said~~ a local processor for execution thereon within ~~said~~ the electronic device;

from outside of the electronic device, ~~checking the validity of said protected data, producing a validity signal indicative of whether said protected data is valid, and~~ setting the electronic device into one of a first mode and a second mode;

checking the validity of said protected data and producing a validity signal indicative of said protected data being valid, wherein the checking and producing steps are performed when the said electronic device is in one of said first mode and said second mode;

inhibiting an output of said validity signal to outside ~~said~~ the electronic device while in said first mode, the electronic device remaining in said first mode until the validity of a predetermined quantity of said protected data has been checked;

resetting the system including at least said local processor; and

resetting said ~~validation~~ validity signal in response to resetting the system while the electronic device is in said first mode, wherein said validity signal is not reset in response to resetting the system while the electronic device is in said second mode.

27. **(Canceled)**

28. **(Canceled)**

32. **(Canceled)**

2. The following is an examiner's statement of reasons for allowance. The present invention is directed to a system and method for controlling output of a validity signal calculated based on memory contents stored in an electronic device wherein the validity signal being reset in response to a system reset. More specifically, independent claims 1 and 20 identify the uniquely distinct features: a device reset function for resetting said validity signal in response to said system being reset while the electronic device is in said first mode, wherein said device reset function does not reset said validity signal in response to said system being reset while the electronic device is in said second mode. The closest prior art, Milios et al (5,860,099), discloses a method for calculating a validity signal (e.g., signature) of memory contents in a controller. Another prior art, Little et al (6,219,789), discloses resetting a validity signal in response to all resets. However, Milios and Little, either alone or in combination, do not teach that the validity signal is reset in response to a system reset while the electronic device is in a first mode and that the validity signal is not reset in response to a system reset while the electronic device is in a second mode. The prior art, taken either singly or in combination, fails to anticipate or fairly suggest the limitations of applicant's independent claim, in such a manner that a rejection under 35 U.S.C 102 or 103 would be proper. The claimed invention is therefore considered to be in condition for allowance as being novel and nonobvious over prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Dinh whose telephone number is 571-272-3802. The examiner can normally be reached on Mon-Fri: 10:00am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MD

Minh Dinh
Examiner
Art Unit 2132

MD
12/23/05

THOMAS R. PEESO
PRIMARY EXAMINER